Claims 1-22 are pending in this case. Claims 1, 19, and 21 have been amended herein. Claim 19 was amended in response to an objection in the last office action and Claims 1 and 21 were amended to correct typographical errors.

New formal drawings were required. New formal drawings accompany this response.

Claims 1, 3, 4, 7-8, 11-13, and 15-22 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Moyer et al. (U.S. Patent No. 4,803,540) in view of Shibata (U.S. Patent No. 6,229,199) and further in view of Brown (U.S. Patent No. 6,148,673) and further in view of Wark et al. (U.S. Patent No. 5,929,521) and further in view of Haehn et al. (U.S. Patent No. 6,261,870). Applicant respectfully traverses the rejection as follows. Claim 1 is to a test socket for a semiconductor device. Neither Moyer nor Shibata nor Brown nor Haehn are even remotely related to test sockets. Wark is only remotely related to that subject. One skilled in the art of test sockets or of semiconductor devices would have received no motivation to combine these disparate and mutually unrelated references. Therefore, Applicant respectfully submits that Claim 1 and Claims 3, 4, 7-8, 11-13, and 15-17 which depend from Claim 1, are patentable over the cited combination of references.

In addition, Applicant respectfully submits that the cited combination is deficient in teaching or suggesting the invention described in Claim 1 even if one assumes for the sake of argument that the skilled artisan would be somehow motivated to combine these five references. It was asserted in the office action that Moyer discloses in Figures 2-5 a "guidepost" as that term is used in Claims 1 and 21, for example. Applicant disagrees. First, Moyer's disclosure pertains to a lead frame, an integral part of a semiconductor device, not to a test socket for a semiconductor device as described in Claim 1 nor to a method of testing a semiconductor device as described in Claim 21. Second, the lead frame is essentially two-dimensional and is very thin in cross-section. So, even if one wanted to use a lead frame as a test socket or in a method of testing, nothing on

the lead frame 13 shown in Figure 2 or elsewhere in Figures 3-5 can reasonably be characterized as a post of any sort in view of the two-dimensional nature of the lead frame. The deformation absorbing members all occur within the plane of the lead frame and therefore could not serve as a guidepost.

It was asserted in the office action that Shibata discloses in Figure 1B a chamfered impact base as described in Claim 1. Applicant disagrees. First, Shibata's disclosure pertains to a method of bonding a semiconductor device to a lead frame. Shibata does not disclose anything relating to a test socket for a semiconductor device. Second, element 12c in Shibata's Figure 1B is a bond wire, not a chamfered impact base. See Figure 1A, where element 12 is clearly shown to be a bond wire. The paragraph in column 2, at line 42 of Shibata is a description of the angle between the bond wire 12 and lead 13 (a part of the lead frame). This has nothing to do with a chamfered impact base.

It was asserted in the office action that Brown discloses in Figure 1, and at column 4, lines 23-46, a floating flag coming into contact with a semiconductor device to alleviate pressure from the device. This citation is assumed to be directed at the floating base feature of Applicant's Claim 1. If so, Applicant disagrees. First, Brown pertains to a differential pressure sensor. Brown does not teach or suggest anything relating to a test socket for a semiconductor device. Second, Brown's references to a "floating" flag are unclear. In column 6, lines 24-27, Brown says that "[b]reaktabs 16 provide an isolating mechanism for mounting flag 14 and allow mounting flag 14 to float after singulation of pressure sensor 30 from dambar 70." However, in column 3, lines 46-48, Brown says that "[m]olded housing 12 serves to hold leadframe 60 components mounting flag 14, lead 18, and breaktab 16 in place and provides a housing and interconnnect for sensor die 10." It is unclear how breaktabs 16 allow flag 14 to "float" within housing 12. Note also that flag 14 is not in contact with sensor die 30. Instead, bond surface 26 and gold-germanium sensor layer 28 are interposed between flag 14 and sensor die 30.

It was asserted in the office action that it would be obvious for one skilled in the art to apply Wark's contact structure to both ends of a pogo-pin. Applicant

disagrees. Wark's motivation for developing the disclosed contact structure was to facilitate damage-free contact to a solder ball. Since solder balls occur on a semiconductor device and not on semiconductor test equipment, one skilled in the art would receive no motivation to apply Wark's teachings to both ends of a pogo-pin. Note also that Wark does not disclose the application of his contact structure to pogo-pins.

It was asserted in the office action that Haehn discloses a back panel as described in Claim 1, for example. Applicant disagrees. Haehn pertains to adapting a semiconductor device for failure analysis, it does not pertain to test sockets.

Claim 18 includes the feature of "a plurality of pins each having a series of contact marks, each set of contact marks being of substantially the same pattern and spaced by a predetermined pitch." Of the five references cited above, only Wark deals with anything similar to this claimed feature. The Wark disclosure, however, discusses minimizing damage to solder balls during probing. Wark does not teach or suggest a semiconductor device including a plurality of ***pins*** each having a series of contact marks. None of the other cited references cure this deficiency of Wark. Therefore, Applicant respectfully submits that Claim 18, as well as Claims 19 and 20 which depend therefrom, are patentable over the cited combination.

Claim 21 is a method for testing a semiconductor device having a plurality of pins including the step of providing a test socket. Neither Moyer, nor Shibata, nor Brown, nor Wark, nor Haehn teach or suggest a method for testing a semiconductor device which includes the step of providing a test socket. Moreover, none of the cited references teach or suggest using a test socket having a plurality of guideposts integrally formed within the body of the socket. Therefore, Applicant submits that Claim 21, as well as Claim 22 which depends therefrom, are patentable over the cited references.

Claim 2 stands rejected under 35 U.S.C. 103(a) as being unpatentable over Moyer in view of Shibata and further in view of

Wark and further in view of Haehn, as applied to Claim 1, and further in view of Kim, et al. (U.S. Patent No. 5,939,776). Claim 2 depends from Claim 1, which Applicant has submitted above to be patentable over Moyer in view of Shibata in view of Brown in view of Wark in view of Haehn. Kim does nothing to cure the deficiencies of the above-cited combination. As with the above references, Kim has nothing to do with test sockets, instead addressing a lead frame structure. One skilled in the art would receive no motivation to combine the teaching of the above-cited references with Kim to obtain the inventions described in Claim 1 or Claim 2. Therefore, Applicant respectfully submits that Claim 2 is patentable over the cited references.

Claims 5, 6, 9, 10, and 14 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Moyer in view of Shibata and further in view of Brown and further in view of Wark and further in view of Haehn, as applied to Claim 1, and further in view of Yerman, et al. (U.S. Patent No. 4,716,124). Claims 5, 6, 9, 10, and 14 depend from Claim 1, which Applicant has submitted above to be patentable over Moyer in view of Shibata in view of Brown in view of Wark in view of Haehn. Yerman does nothing to cure the deficiencies of the above-cited combination. In fact, Yerman teaches away from such a combination by teaching the use of a tape-based test method instead of using a test socket as described in Claim 1. Therefore, Applicant respectfully submits that Claim 1, as well as Claims 5, 6, 9, 10, and 14 which depend therefrom, are patentable over the above-cited references further in view of Yerman.

In view of the above, Applicant respectfully requests withdrawal of the rejections and allowance of claims 1-22. If the Examiner has any questions or other correspondence regarding this application, Applicant requests that the Examiner contact Applicant's attorney at the below listed telephone number and address.

Respectfully submitted,

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Claims

1. (amended) A test socket for a semiconductor device having a plurality of pins, the test socket comprising:

a body for receiving a semiconductor device, the body having an integrally formed guidepost and a chamfered impact base;

a floating base disposed within the body, the floating base coming into contact with the semiconductor device and providing movement of the semiconductor device to alleviate unwanted pressure from the plurality of pins;

a plurality of pogo-pins adjacent to one another, each pogo-pin comprising a cylindrical chamber and a plunger having a crown top at both ends, one end for directly contacting a pin of the semiconductor device and the other end for contacting external test equipment; and

a back panel removably attached to the body.

19. (amended) The semiconductor device of Claim 18 [17] wherein a series of sets of contact marks result from the testing of the semiconductor device in a test socket comprising a plurality of pogo-pins having a crown portion with pointed ends for directly contacting the plurality of pins of the semiconductor device, the pointed ends having the predetermined pitch.

21. (amended) A method of testing a semiconductor device having a plurality of pins, the method comprising:

providing a test socket having a body for receiving a semiconductor device, the test socket including a plurality of guide posts [guidepost] integrally formed within the body and a plurality of pogo-pins adjacent to one another for directly contacting the plurality of pins;

aligning the semiconductor device within the body utilizing the guide posts;

applying a pressure which brings the plurality of semiconductor device pins into contact with the plurality of pogo-pins; and

testing the semiconductor device.